BASIC ELECTRONICS ENGINEERING

(RBL1B002)

MODULE-1

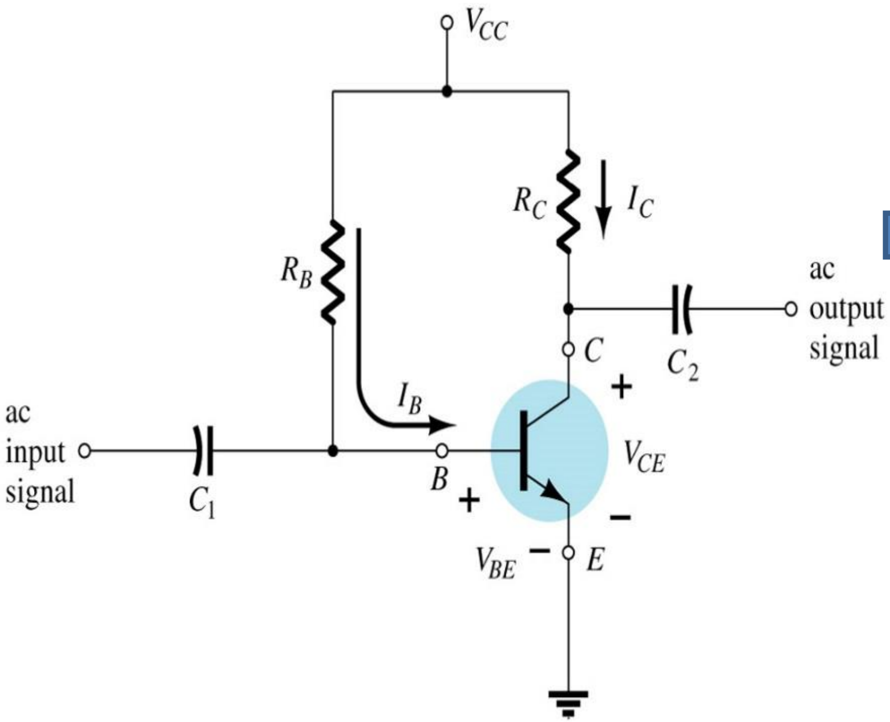
BJT DC BIASING

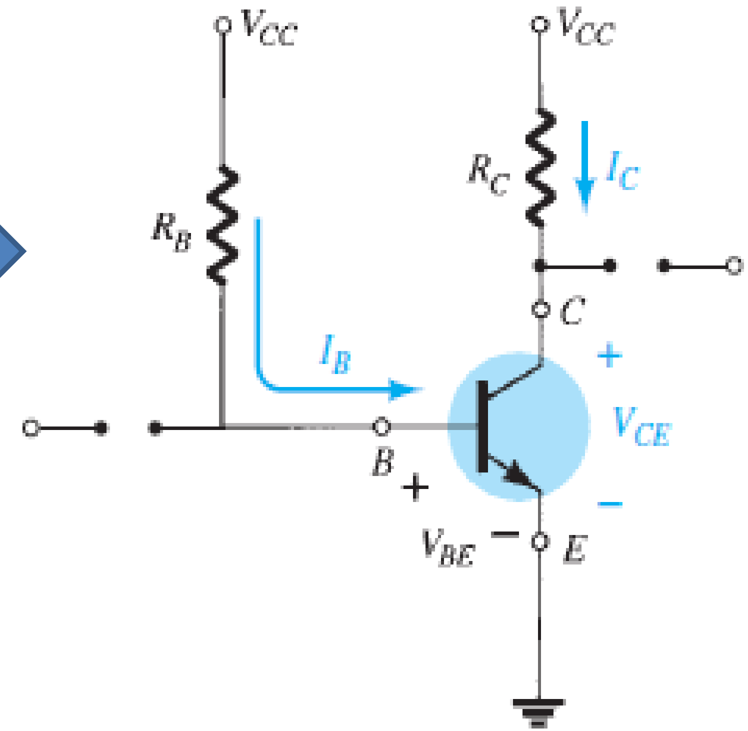
- 4 types of biasing circuits are there.
  - Fixed Bias Circuit
  - Emitter Stabilized Bias Circuit
  - Voltage Divider Bias Circuit
  - DC bias with voltage feedback

NOTE:

1. $I_E = I_B + I_C$
2. $\beta = \frac{I_C}{I_B}$
3. $I_E \approx I_C$
4. $V_{BE} = \begin{cases} 0.7 \; for \; Si \\ 0.3 \; for \; Ge \end{cases}$
5. $V_{XY} = V_X - V_Y$

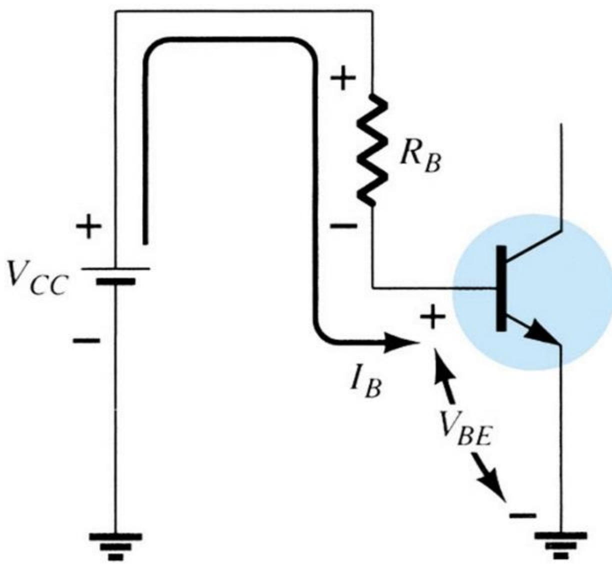
Fixed Bias Circuit





Fixed Bias Circuit

Base-Emitter Loop



Using Kirchoff's voltage law:

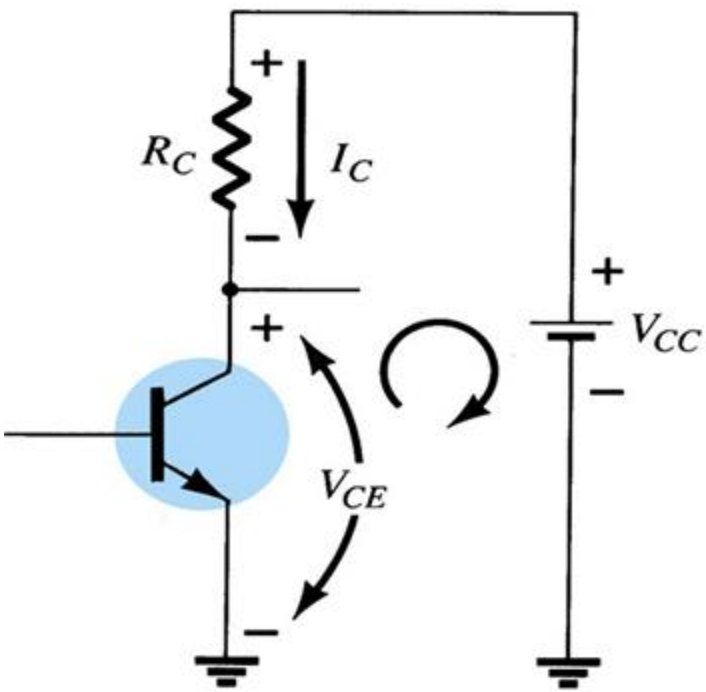
$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for I_B :

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Fixed Bias Circuit

Collector-Emitter Loop



Using Kirchoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$

We know that

$$V_{CE} = V_C - V_E$$

Since $V_E = 0$ V, then:

$$V_{CE} = V_C$$

Also we know that :

$$V_{BE} = V_B - V_E$$

Since $V_E = 0$V, then:

$$V_{BE} = V_B$$

Load Line Analysis - Fixed Bias Circuit

The load line is a straight line which is used to locate the optimum biasing or operating point of a nonlinear device. The intersection of the dc bias value of I_B with the dc load line determines the *Q*-point

The CE loop of the fixed bias circuit:

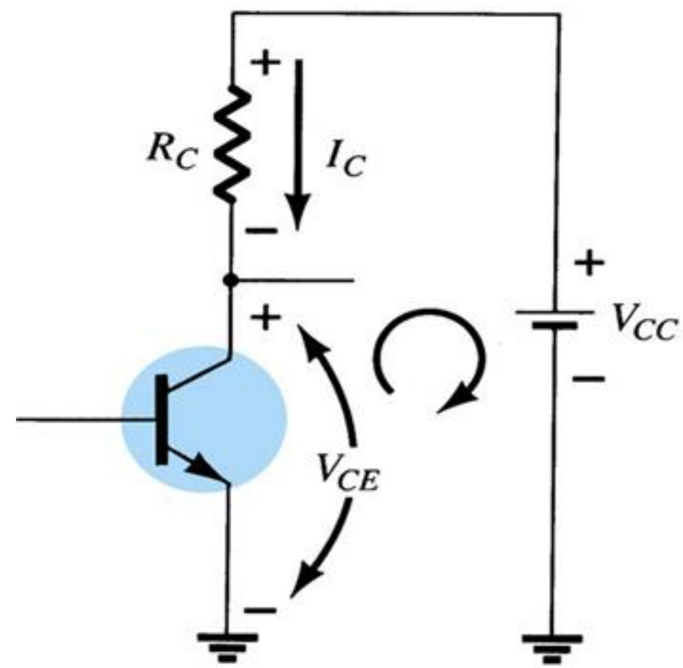
By KVL:

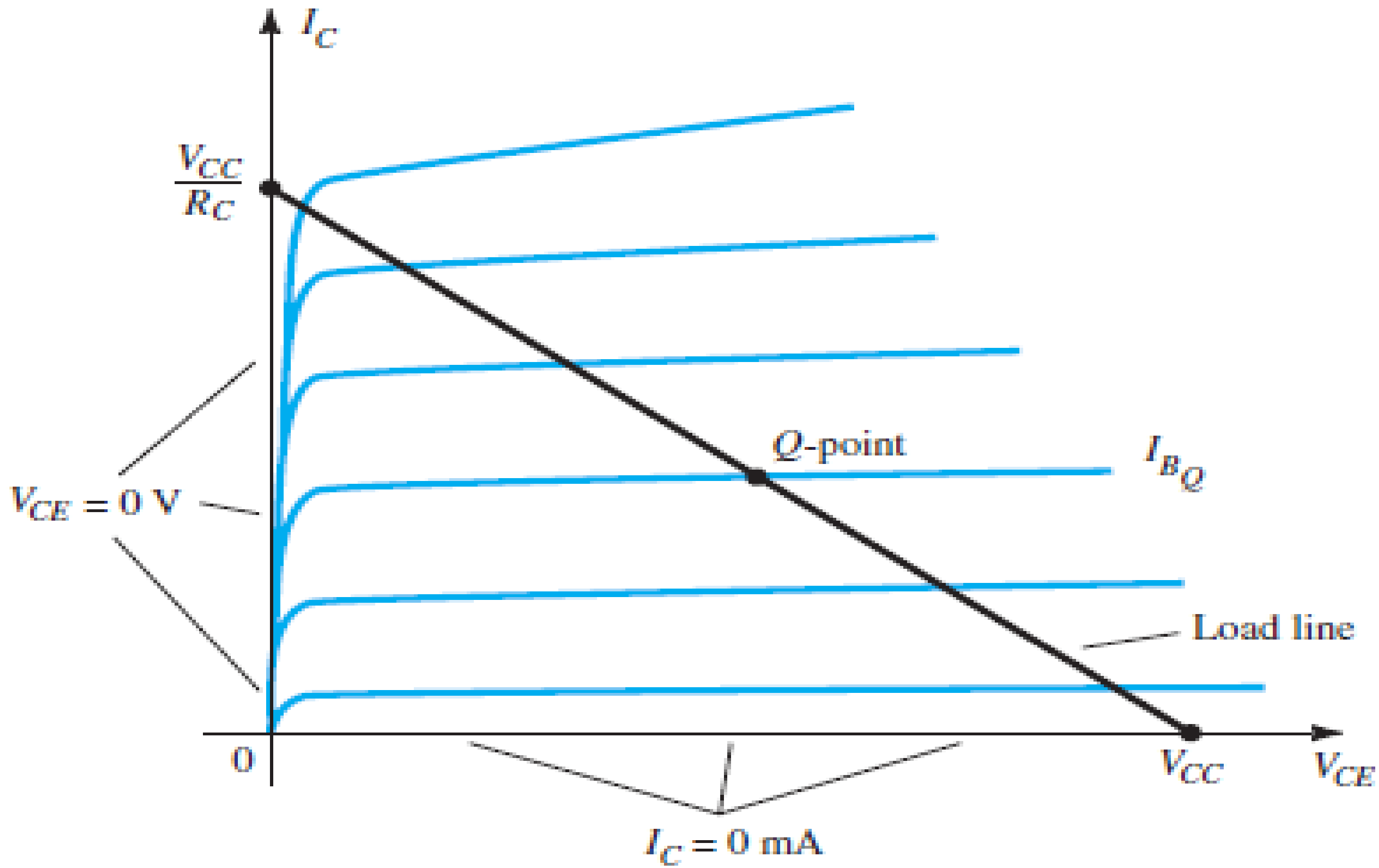
$V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C R_C$

Let $I_C = 0$, So $V_{CE} = V_{CC}$

Again, let $V_{CE} = 0$, So $I_C = V_{CC} / R_C$





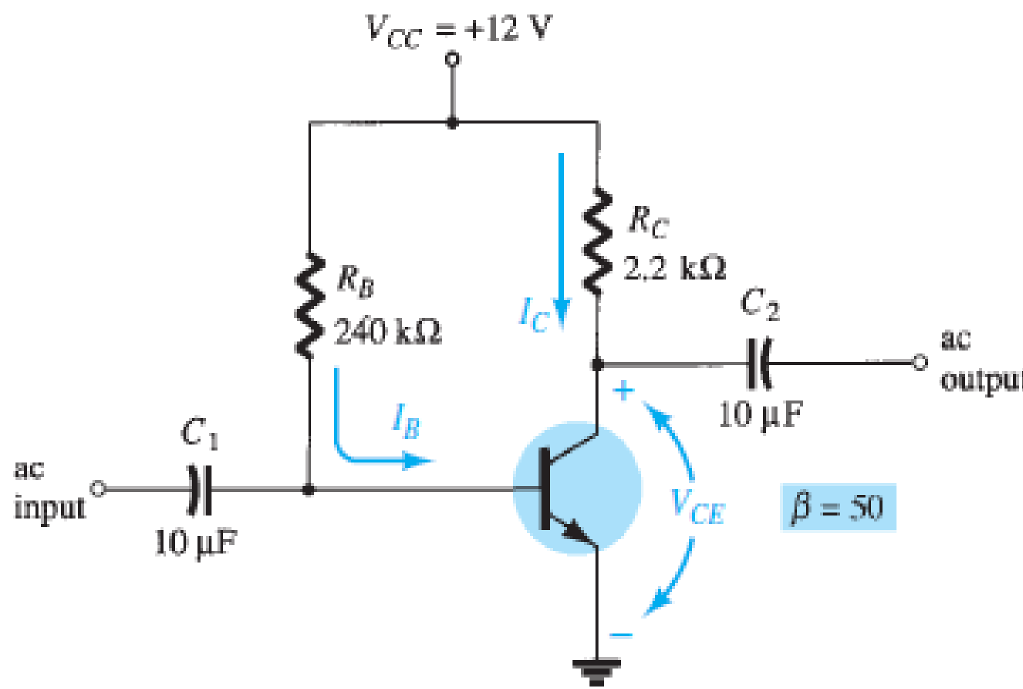
I_C
$\frac{V_{CC}}{R_C}$
$V_{CE} = 0$ V
Q-point
I_{B_Q}
Load line
0
V_{CC}
V_{CE}
$I_C = 0$ mA

Fixed Bias Circuit

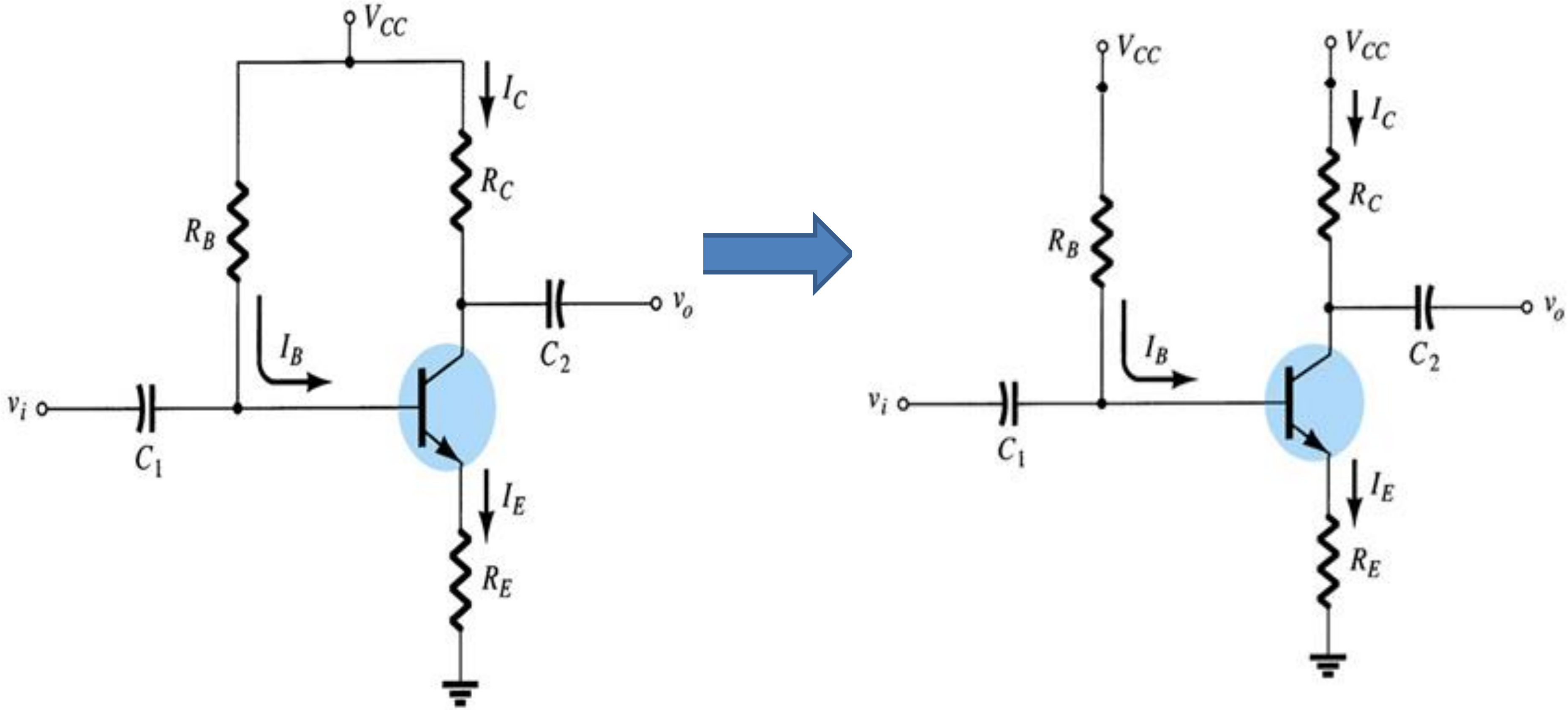
PRACTICE:

Determine the following for the fixed bias configuration.

- I_{BQ}, I_{CQ}
- V_{CEQ}
- V_B and V_C
- V_{BC}

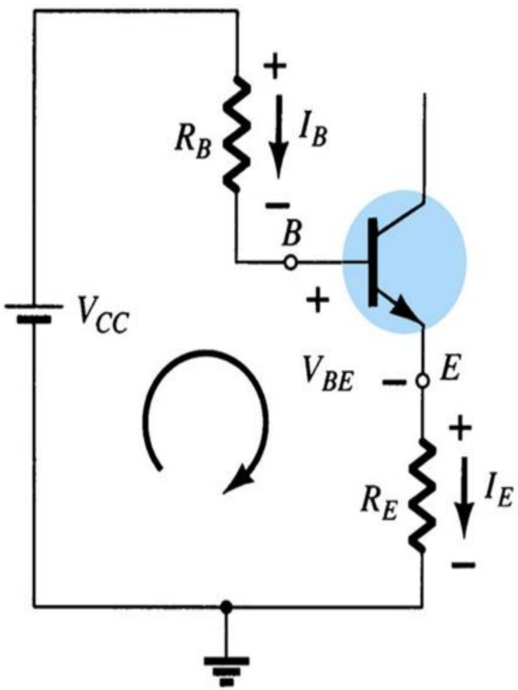


Emitter Stabilized Bias Circuit



Emitter Stabilized Bias Circuit

Base-Emitter Loop



Applying KVL: $+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

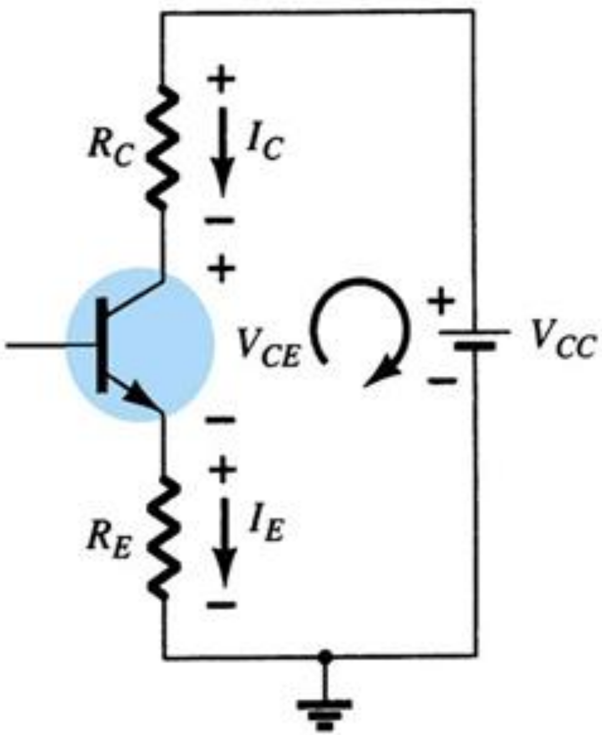
Knowing: $I_E = (\beta + 1) I_B$

We have: $+V_{CC} - I_B R_B - V_{BE} - (\beta+1) I_B R_E = 0$

Solving for I_B: $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Emitter Stabilized Bias Circuit

Collector-Emitter Loop



Applying KVL: $+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$

Knowing that $I_E \cong I_C$ and solving for V_{CE} :

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Finding V_E: $V_E = I_E R_E$

Finding V_C: $V_C = V_{CE} + V_E$ or $V_C = V_{CC} - I_C R_C$

Finding $V_B = V_{BE} + V_E$ or $V_B = V_{CC} - I_B R_B$

Emitter Stabilized Bias Circuit

Improved Bias Stability

The addition of the **emitter resistor** to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.

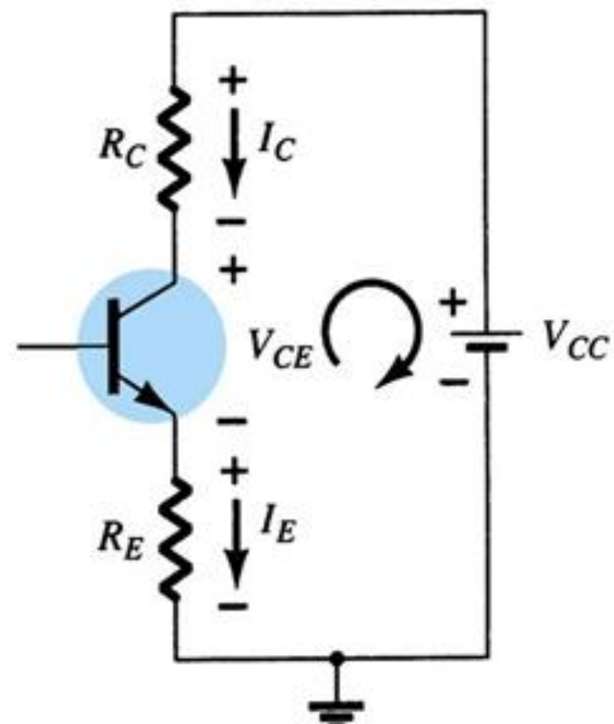
Load Line Analysis – Emitter Stabilized Bias Circuit

The CE loop of the fixed bias circuit:

By KVL:

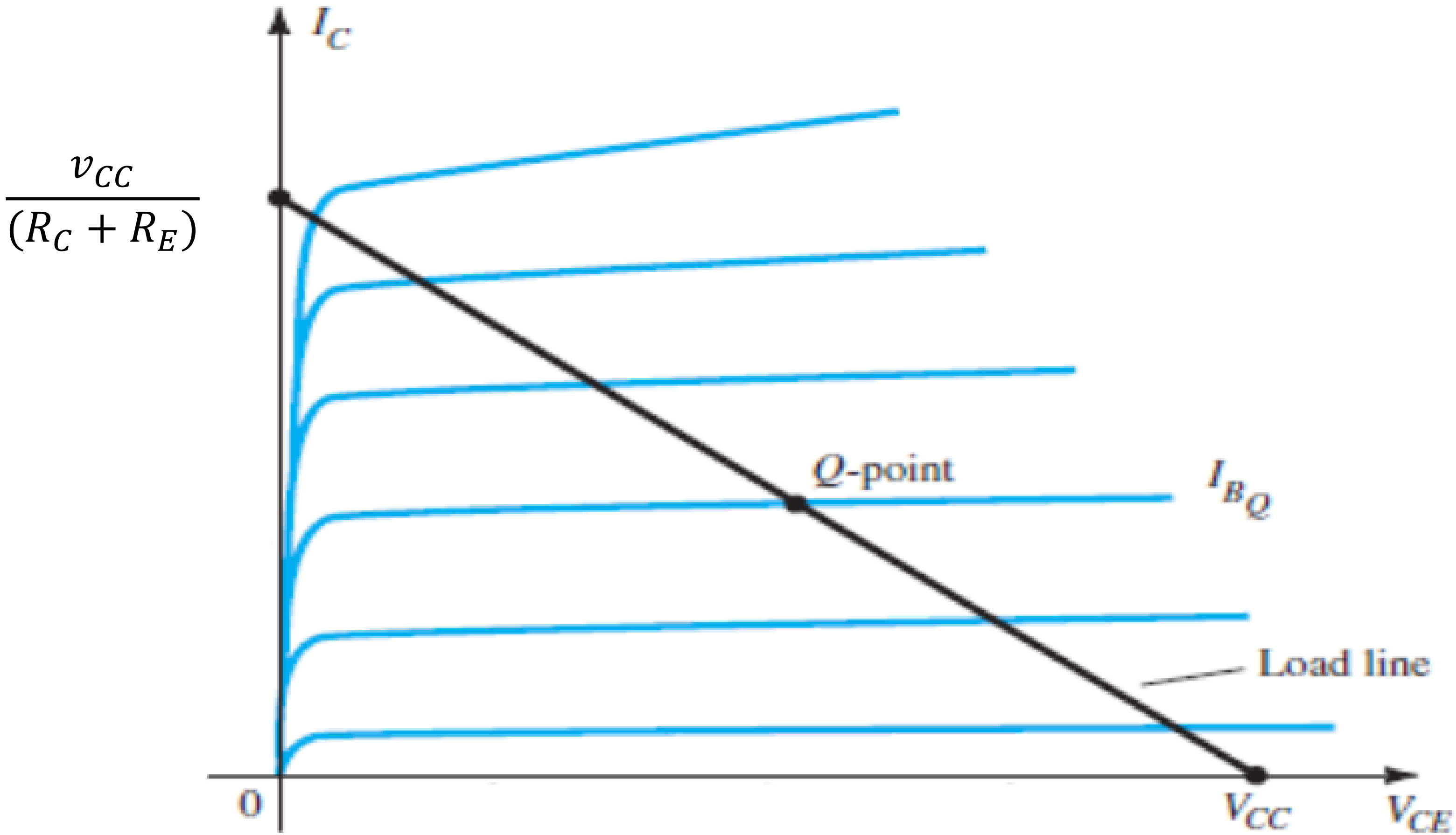
$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$

$\Rightarrow V_{CE} = V_{CC} - I_C\,(R_C + R_E)$



Let $I_C = 0$, So $V_{CE} = V_{CC}$

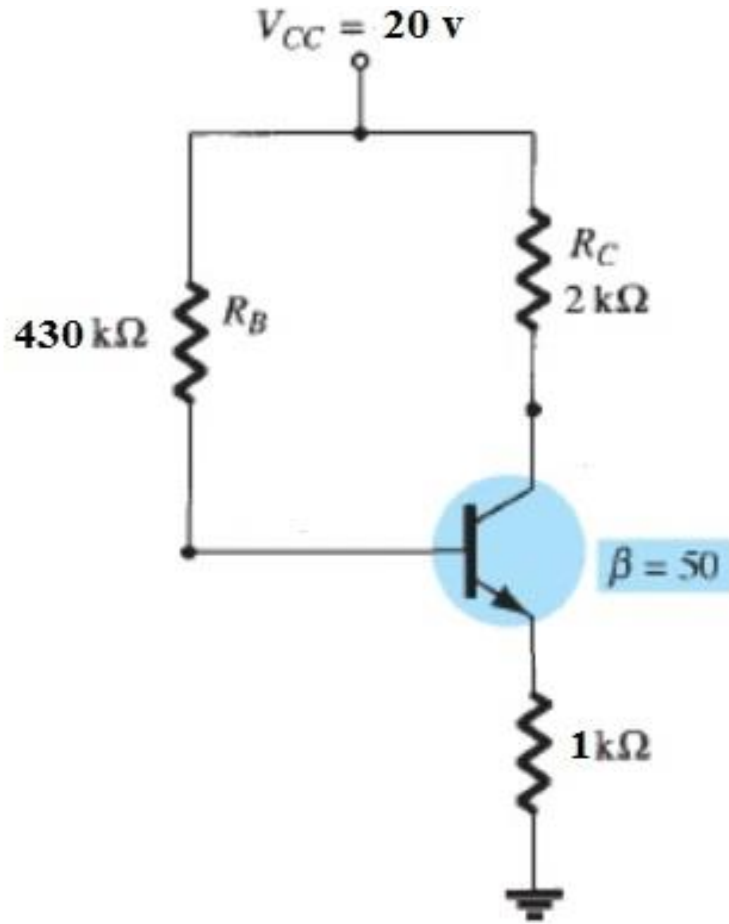
Again, let $V_{CE} = 0$, So $I_C = V_{CC} / (R_C + R_E)$



I_C
$\frac{v_{CC}}{(R_C + R_E)}$
Q-point
I_{B_Q}
Load line
0
V_{CC}
V_{CE}

PRACTICE

Emitter Stabilized Bias Circuit



Determine the following for the given circuit for β = 50

(a) I_B

(b) I_C

(c) V_{CE}

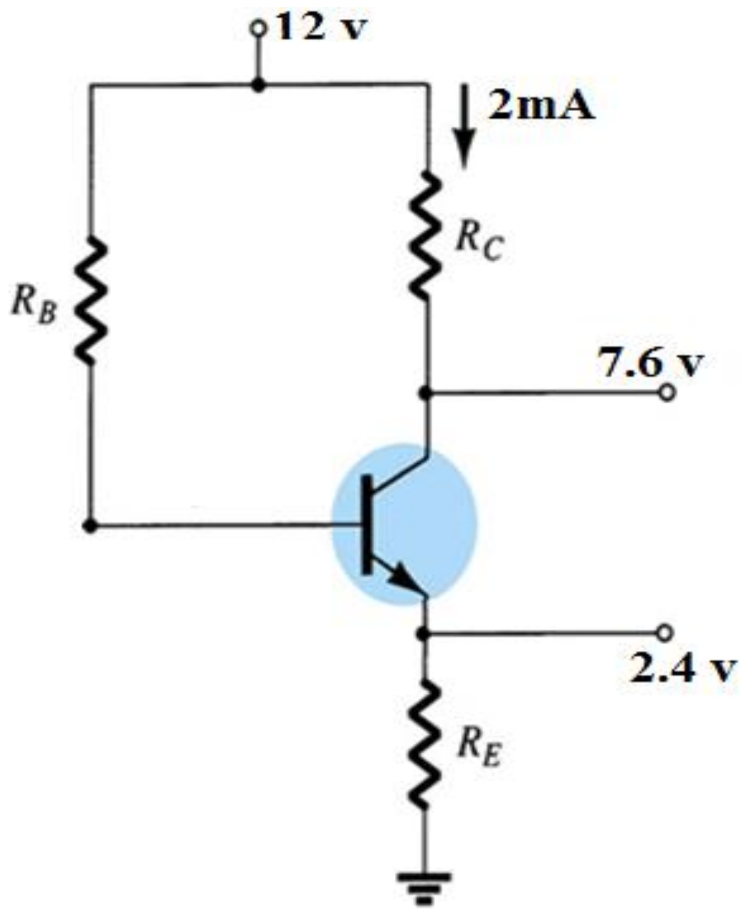
(d) V_C

(e) V_E

(f) V_B

(e) V_{BC}

Emitter Stabilized Bias Circuit



Determine the following for the given circuit for $\beta = 80$

(a) R_C

(b) R_E

(c) R_B

(d) V_{CE}

(e) V_B